[11] R. Sung, P. Bendix, and M. B. Das, "Extraction of high-frequency equivalent circuit parameters of submicron gate-length MOSFET's," *IEEE Trans. Electron Devices*, vol. 45, pp. 1769–1775, Aug. 1998.
[12] J.-P. Raskin, R. Gillon, J. Chen, D. Vanhoenacker-Janvier, and J.-P. Colinge, "Accurate SOI MOSFET characterization at microwave frequencies for device performance optimization and analog modeling," *IEEE Trans. Electron Devices*, vol. 45, pp. 1017–1025, May 1998.
[13] T. M. Roh, Y. Kim, Y. Suh, W. Sang Park, and B. Kim, "A simple and accurate MESFET channel-current model including bias-dependent dispersion and thermal phenomena," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 1252–1255, Aug. 1997.

A Low-Cost Uniplanar Sampling Down-Converter with Internal Local Oscillator, Pulse Generator, and IF Amplifier

Jeong S. Lee and Cam Nguyen

***Abstract*—In this paper, we report on the development of a new integrated-circuit sampling down-converter having its own pulse generator, local oscillator (LO), and IF amplifier. The internal pulse generator uses a step recovery diode together with a unique ultra-wide-band hybrid junction to generate sub-nanosecond balanced pulses for gating the sampling diodes. The down-converter exhibits a conversion gain from 12 to 15.5 dB over an RF frequency of 0.01–3 GHz with 10-MHz LO and sampling pulses of about 100 ps. Return loss at the RF port is better than 15 dB over this RF bandwidth. The down-converter exhibits a good linearity and low harmonic levels. This down-converter employs a coplanar waveguide and slot line to make the entire circuit uniplanar and is, thus, suitable for low-cost production. In addition, it has an internal pulse generator, LO, and IF amplifier, making it a compact receiver subsystem, which can readily be used in many microwave systems.**

***Index Terms*—MIC, mixer, receiver, sampler, uniplanar circuit.**

I. Introduction

A sampling down-converter is an important component in many systems such as sampling oscilloscopes, microwave counters, phase-locked instruments, and radar [1]–[5]. In particular, compact and low-cost sampling down-converters are very desirable. Existing sampling down-converters use a combination of planar and uniplanar transmission lines, requiring two-sided circuit processing, which results in high complexity and fabrication cost. Completely uniplanar sampling down-converters, in which all of the circuit elements are located on one side of the substrate, are highly desired for simplicity and low cost. These unique advantages are attained because uniplanar structures allow ease in mounting solid-state devices, elimination of via holes, and only one-sided circuit processing.

In this paper, we describe a new integrated-circuit sampling down-converter using sequential or coherent sampling. This sampling scheme, having a relatively low sampling rate, is generally used in pulsed surface penetrating radar. This down-converter has its own local oscillator (LO), pulse generator, and IF amplifier, making it a complete receiver subsystem. It is completely fabricated using a (uniplanar) coplanar waveguide (CPW) and slot line. In addition, novel configurations for the sampling head and pulse generator are used to achieve less-distortion sampling pulses and high conversion gain by exploiting the combined advantages of a CPW and slot line. The sampling head of the down-converter uses a two-diode sampling bridge to make a balanced structure for good inter-port isolations and cancellation of AM noise from the LO. The pulse generator employs a step recovery diode (SRD) and an ultra-wide-band hybrid junction to create two opposite pulses for gating (or turning on/off) the sampling diodes. In the first design, we achieve a conversion gain of 12–15.5 dB over 0.01–3-GHz RF bandwidth with 10-MHz LO and 100-ps sampling pulses. More than 15-dB RF return loss has also been measured. The down-converter has good linearity and harmonic rejection.

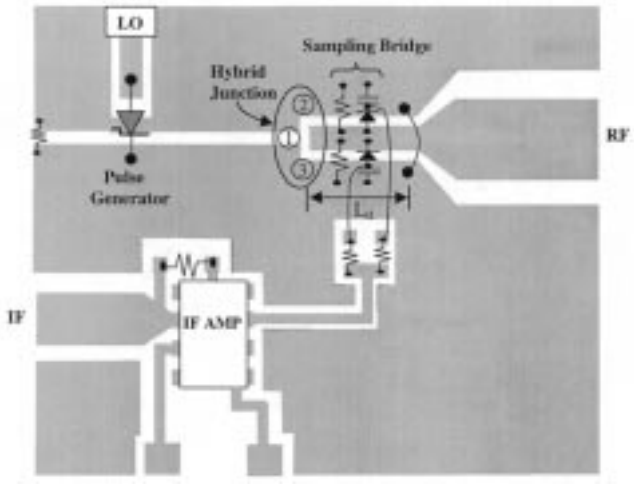

Fig. 1. Layout of the sampling down-converter.

II. Circuit Design

Fig. 1 shows the layout of the sampling down-converter, consisting of a sub-nanosecond pulse generator, hybrid junction, sampling head, LO, and IF amplifier. The main components are the pulse generator, hybrid junction, and sampling head. The pulse generator generates a step function from the LO signal, which is then fed to the hybrid junction to produce two opposite pulses for gating the sampling diodes. The sampling head is used to sample, hold, and convert the RF signal into an IF signal. They are described in details as follows.

A. Sub-Nanosecond Pulse Generator and Hybrid Junction

Pulse generators have been developed using microstrip lines and SRDs [2], [4]. SRDs are perhaps the most commonly used devices for pulse generation. Its theory is given in details in [6]. Nonlinear transmission line implemented using a CPW and an SRD has also been used to generate a sharp-edge pulse [7]. Our sub-nanosecond pulse generator also uses an SRD, but we combine a CPW and a slot line to achieve circuit simplicity, less distortion, and ready interface with the LO and sampling head of the down- converter. These uniplanar structures also permit simple connection for the SRD.

A 10-MHz square-wave LO signal is fed to the SRD, via a 50-Ω CPW, to generate a step function. This step function divides into two

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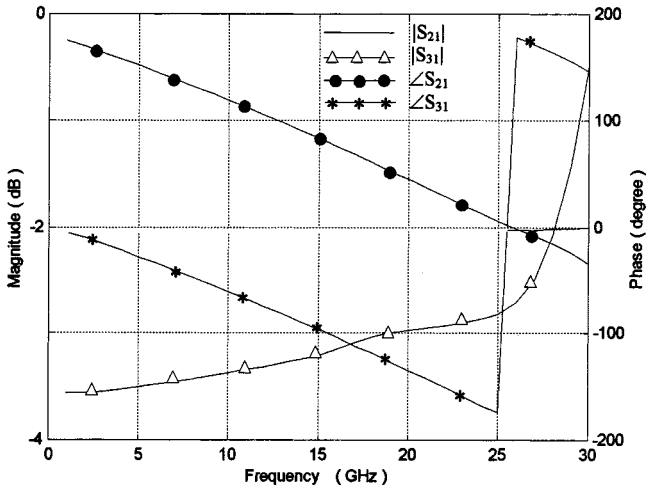

Fig. 2. Calculated amplitudes and phases of S_{21} and S_{31} of the hybrid junction.

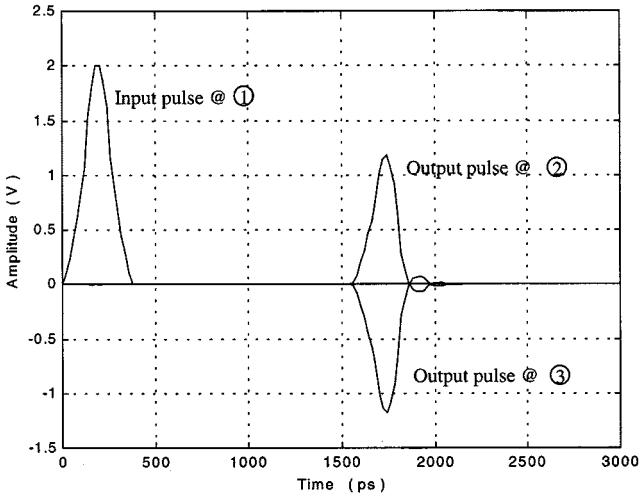

Fig. 3. Calculated time-domain response of the hybrid junction.

step functions upon arriving at the slot line. One step function propagates toward the slot line's end terminated by a resistor whose value equals to the slot line's characteristic impedance, and is absorbed. The other step function travels along the other slot line's portion toward the hybrid junction and, upon reaching the junction, splits into two step functions of equal amplitudes and opposite phases. These step functions then propagate along the two slot lines and are reflected back to the hybrid junction by an air bridge across the two ground planes. The reflected step functions arrive at the hybrid junction after a certain time and combine with other incident step functions to form two pulses at the two slots of the hybrid junction. The air bridge is used to simulate a short circuit to the slot mode, under which the step functions propagate. It is located at a distance of L_d from the hybrid junction, which approximately determines the width of the pulse produced at each hybrid junction's slot as

$$t_g = \frac{2L_d}{u_p} \tag{1}$$

where u_p is the phase velocity.

The hybrid junction, as seen in Fig. 1, is realized by single and coupled slot lines. It should be noted that this hybrid junction, used for creating two balanced pulses, operates based on the principles of balanced single and coupled slot lines. Therefore, the step functions, after emerging from the hybrid junction, propagate as slot modes in the two slot lines, as noted earlier. This hybrid junction has a unique field distribution that allows an input pulse to be divided into two balanced pulses of opposite polarity with minimum pulse distortion. The very small distortion is achieved because the field behavior of this structure is almost frequency independent, resulting in an extremely wide bandwidth. Other ways of realizing balanced pulses, such as [4], causes more signal distortion because of limited bandwidths of the baluns used. Fig. 2 shows the magnitudes and phases of S_{21} and S_{31} of the hybrid junction, calculated using the Momentum program,[1] with the input port 1 and output ports 2 and 3 located 0.2 in away from the junction. With reference to 3-dB insertion loss, this hybrid junction shows a very wide-band balun characteristic with amplitude and phase balances of almost 0° and 180°, respectively, from 0.1 MHz up to about 25 GHz. Fig. 3 shows the time-domain simulation results of the hybrid junction using the Libra program.[2] The output pulses resemble closely the input pulse with reduced amplitudes and are 180° out of phase with respect to each other.

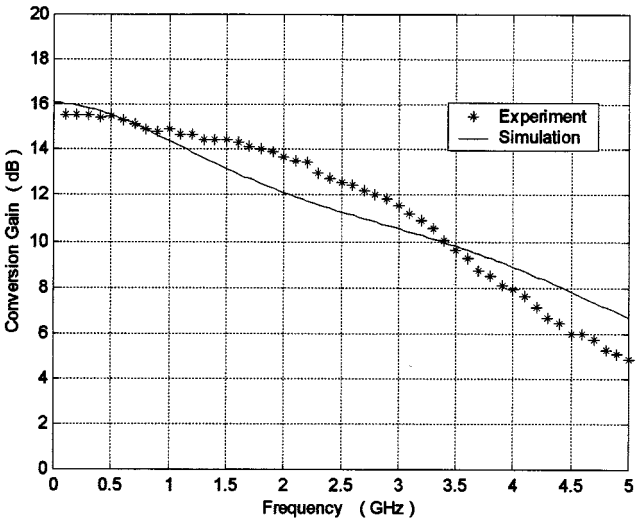

Fig. 4. Conversion gain of the sampling down-converter.

B. Sampling Head

The sampling head contains a sampling bridge, which is comprised of two identical parts (see Fig. 1). Each part has a Schottky sampling diode, holding capacitor, and terminating resistor, mounted across one output slot of the hybrid junction. The two parts of the sampling bridge appear in series with respect to the LO port and in parallel with respect to the RF and IF ports. The sampling capacitance substantially affects the bandwidth of the sampling circuit, with a smaller sampling capacitance producing a wider bandwidth. Finding the exact bandwidth of the sampling circuit is complicated with gating-time duration, pulse

[1]Hewlett-Packard Company, Advanced Design System, version 1.1, Santa Rosa, CA, 1999.

[2]Hewlett-Packard Company, Advanced Design System, version 1.1, Santa Rosa, CA, 1999.

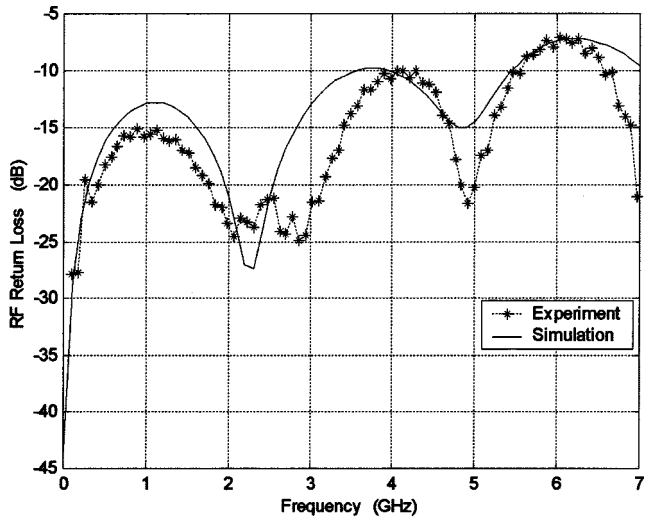

Fig. 5. RF return loss of the sampling down-converter.

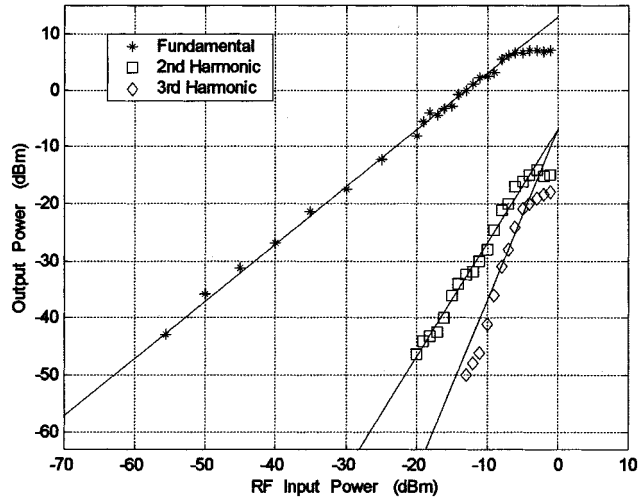

Fig. 6. Output powers of the sampling down-converter versus RF input power at 1.5 GHz.

rise time, reflection, and high-frequency effects. However, an approximate bandwidth can be determined as [1]

$$B \cong \frac{350}{t_s} \text{ GHz} \tag{2}$$

where t_s is the sampling pulsewidth (in picoseconds).

Note that while the balanced pulses, which sample the sampling head, propagate as a (balanced) slot-line mode, the RF and IF signals travel as a (unbalanced) CPW mode. This leads to inherent isolations between LO/RF and LO/IF.

III. Circuit Fabrication and Performance

Fig. 1 is the layout of the complete integrated-circuit sampling down-converter including the LO and IF amplifiers. All the elements are located on only one side of the substrate. Both the input and output ports are CPW and, thus, are readily interfaced with external components. The sampling down-converter was fabricated on an RT/Duroid 6010 substrate with a relative dielectric constant of 10.2 and a thickness of 0.050 in. The sampling diodes used are Hewlett-Packard HSCH-5531 beam-lead Schottky diodes having junction and package capacitances of about 0.2 and 0.1 pF, respectively. The SRD is MMD-0840 (Metelic Company, Sunnyvale, CA), which has a nominal lifetime of 10 ns, 75-ps transition time, and 0.6-pF junction capacitance. A 2-pF chip capacitor and 100-Ω chip resistor are used as the sampling capacitor and terminating resistor, respectively. The LO is a crystal oscillator that generates a square wave of 10-MHz repetition rate with a good frequency stability and low phase noise. The IF amplifier is an analog operational amplifier.

Simulation of the sampling down-converter was performed using both the Momentum and Libra programs. Fig. 4 displays the measured and calculated conversion gains of the down-converter versus RF frequency, showing more than 12-dB gain over a 3-dB bandwidth of almost 3 GHz. The down-converted IF signal is about 11 kHz. Fig. 5 shows the measured and calculated return losses at the RF port. The measured return loss is more than 15 dB up to 3.5 GHz. As seen in Figs. 4 and 5, the measured and calculated results agree reasonably well. Fig. 6 shows the measured powers of the fundamental, second, and third harmonics of the output IF signal versus RF input power at 1.5 GHz, which were sampled at a 10-MHz rate. This figure also illustrates typical output linearity and harmonic response of the down-converter. It should be noted that these results were obtained with the first design of the down-converter.

IV. Conclusions

A new uniplanar sampling down-converter including pulse generator, LO, and IF amplifier has been developed. A conversion gain between 12–15.5 dB, when the RF sweeping from 0.01 to about 3 GHz was sampled at 10-MHz rate with sampling pulses of about 100 ps, has been measured. More than 15-dB return loss at the RF port has also been achieved over this RF bandwidth. The down-converter exhibits good linearity and harmonic suppression. The calculated and measured voltage gains and RF return losses also agree reasonably well. These results were achieved with the first down-converter design. The uniplanar structure of this down-converter makes it attractive for compact low-cost applications. The developed down-converter is a complete receiver subsystem and, therefore, can readily be used in various microwave systems such as an ultra-wide-band surface penetrating radar.

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References

[1] W. M. Grove, "Sampling for oscilloscopes and other RF systems DC through X-band," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-14, pp. 629–635, Dec. 1966.
[2] S. R. Gibson, "Gallium arsenide lowers cost and improves performance of microwave counters," *Hewlett-Packard J.*, pp. 4–10, Feb. 1986.
[3] C. Yen, "Phased-locked sampling instruments," *IEEE Trans. Instrum. Meas.*, vol. IM-14, pp. 64–68, Mar.–June 1965.
[4] K. Madani *et al.*, "A 20-GHz microwave sampler," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 1960–1963, Oct. 1992.
[5] D. J. Daniels, *Subsurface-Penetrating Radar*. London, U.K.: IEE Press, 1996, ch. 5.
[6] J. L. Moll *et al.*, "Physical modeling of the step recovery diode for pulse and harmonic generation circuits," *Proc. IEEE*, vol. 57, no. 7, pp. 1250–1259, July 1969.
[7] M. J. W. Rodwell *et al.*, "GaAs nonlinear transmission lines for picosecond pulse generation and millimeter-wave sampling," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 1194–1204, July 1991.